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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,244	03/23/2004	Motohiro Enkaku	250923US2S	1778

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,244	ENKAKU, MOTOHIRO	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *10,14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/23/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are present for examination.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date (08/29/2003) is being used for this examination.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the application.

Drawings

The drawings (4-6) are objected to since it is unclear to the examiner what values "n" and "k" are representative of with regards to the figures. Additionally figure 25 is objected to since it is unclear to the examiner after review of the figure what is being illustrated, labels other than numerical are requested for understanding. Examiner notes that no other objections to the remaining figures are apparent at this time. Appropriate correction is required for all figures (4-6 and 25) objected to.

Claim Objections

Claims 10,14, and 18 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Examiner notes that this objection is in view of the 35 U.S.C. 112, second paragraph rejection as per claim 8 which these claims are dependent on.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 4, 12, and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Examiner interprets that pages 21-22 of the specification pertain to the claims wherein it is indicated that the mirror-ring register 11' holds the same information as that of register 11 (information holding circuit) wherein is it determined the information is in error. If the information in register 11 is determined to be in error then the information in register 11' would also be in error since they are the same information. This understanding of the specification renders the claims unclear as to how transferring the information mutually between register 11' to register 11 would be a correction process for the information in register 11 making the information between the two registers coincident with each other since they are already the same.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 8 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is:

> A comparison between the compression information compressed and the expected value information so that the information output circuit can output the expected value correction information used to correct the compression information compressed.

Examiner notes that this step is required since without this comparison a value of the expected value correction information is not obtainable and thus not available for output by the information output circuit, without this output the claim could not produce a concrete or repeatable tangible result. Additionally Examiner notes that the compression information compressed can only be compared to expected value information that is also compressed based on the information programmed by the programmable circuit so that a proper comparison can be done.

3. Claims 9-19 are dependent on claim 8 and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claim and may not be further considered on their merits.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA), in view of Shirasake (4287594), and further in view of Fukuda (2001/0054166 A1).

1. As per claim 1, AAPA teaches

A programmable circuit in which information is programmed (page 2 line 24 of the SPEC);

An information holding circuit which electronically holds information programmed in the programmable circuit (page 2 lines 24-25 of the SPEC);

AAPA does not specifically teach:

A compression circuit which compresses information held in the information holding circuit;

An information output circuit which outputs expected value information; and

A detecting circuit which compares the expected value information with compression information of the information compression circuit to check destruction of information held in the information holding circuit.

However those of ordinary skill in the art at the time the invention was made would recognize that to have a compression circuit for compressing information held within the holding circuit, an information output circuit which outputs expected value information, and an detecting circuit which compares expected and compressed information to check for errors within the compressed information are all well known. In an analogous art Fukuda teaches the compression circuitry (Fukuda - paragraph 7 lines 9-11) while in another analogous Shirasaka teaches the output circuitry (Shirasaka - column 1 line 30) and detection circuitry (Shirasaka - column 3 lines 5-10).

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporated a compression circuit for compressing information held within the holding circuit as taught be AAPA to reduce the memory required within the holding circuit to hold the information, thus reducing the complexity, size, transfer time of the information between components, and heat generated within the circuitry. Additionally one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate an information output circuit that outputs expected value information along with a detecting circuit to perform a comparison between expected and compressed information to check for errors within the compressed information to implement parallel processing to reduce processing time.

2. As per claim 6, AAPA as modified teaches wherein the information output circuit includes an expected values information generation circuit which generates expected value information and the expected value information generating circuit compresses information programmed in the programmable circuit to generate expected value

information when the programmed information is held in the information holding circuit (Shirasaka – column 3 lines 5-10).

3. As per claim 7, AAPA as modified teaches the above programmable circuit, information holding circuit, compression circuit, information output circuit, and detecting circuit.

AAPA as modified does not specifically teach wherein the compression process is in accumulative addition process.

However those of ordinary skill in the art at the time the invention was made would recognize that an addition compression process is well know.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to have the compression process be an addition accumulation process since is it a quick and easily implemented process.

Claims 2-4, 8, 9, 11, 12, 15, 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA), in view of Shirasaka (4287594), in view of Fukuda (2001/0054166 A1) as applied to claim 1 above, and further in view of Kang (5958080).

4. As per claims 2, 8, and 9, AAPA as modified teaches the above programmable circuit, information holding circuit, compression circuit, information output circuit, and detecting circuit.

AAPA as modified does not specifically teach comprising a correction process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that the information is destroyed.

However in an analogous art Kang teaches of a correction process execution circuit, which executes a correction process for information held within a holding circuit wherein it is detected that errors or losses in information are present (column 1 lines 36-56).

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to incorporate in AAPA as modified, Kang's correction process execution circuit to correct errors, losses, or destroyed information within information held within a circuit to produce desirable accurate tangible information.

5. As per claims 3, 11, and 15, AAPA as modified with Kang teaches the correction process is a process to transfer information programmed in the programmable circuit to the information holding circuit (Kang - column 1 line 56).

6. As per claims 4, 12, and 16, AAPA as modified with Kang teaches comprising a mirror-ring information holding circuit configured by connecting the information holding circuit in a mirror-ring form,

Wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit (Kang – column 1 lines 53-56).

7. As per claim 18, AAPA as modified teaches wherein the information output circuit includes an expected values information generation circuit which generates expected value information and the expected value information generating circuit compresses

information programmed in the programmable circuit to generate expected value information when the programmed information is held in the information holding circuit (Shirasaka – column 3 lines 5-10).

8. As per claim 19, AAPA as modified teaches the above programmable circuit, information holding circuit, compression circuit, information output circuit, and detecting circuit.

AAPA as modified does not specifically teach wherein the compression process is in accumulative addition process.

However those of ordinary skill in the art at the time the invention was made would recognize that an addition compression process is well know.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to have the compression process be an addition accumulation process since is it a quick and easily implemented process.

Claims 5, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (AAPA), in view of Shirasaka (4287594), in view of Fukuda (2001/0054166 A1), in view of Kang (5958080) as applied to claim 2 above, and further in view of Whetsel (6560734).

9. As per claims 5, 13, and 17, AAPA as modified with Kang teaches comprising a programmable circuit, information holding circuit, compression circuit, information output circuit, detecting circuit, and correction process execution circuit.

AAPA as modified with Kang does not specifically teach an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro,

Wherein the correction process execution circuit suspends a system containing the IP macro when the IP macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status.

However in an analogous art Whetsel teaches of IP macro implementation within ICs which provide a complex circuit function (column 1 lines 23-25). Additionally those of ordinary skill in the art at the time the invention was made would recognize that suspending or resetting a system pending on a required element status is well known in the art.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to implement the IP macro as taught be Whetsel with AAPA as modified with Kang to as Whetsel indicates, quickly provide a complex circuit function within a system (Whetsel – column 1 lines 24-25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven D. Radosevich
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER